CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1-6. (Cancelled).

7. (Currently Amended) An RF power LDMOS transistor comprising:

- a substrate,

- a first and second source region spaced apart**, wherein each source region comprise a first region and a second region surrounding said first region, wherein the second region is less doped than said first region,**

- a sinker separating said first and second source region,

- a first and second drain region arranged to define in combination with said first and second source region a first and second channel,

- a first and second gate finger covering said first and second channel, respectively,

- first and second metal clamps which short-circuit the sinker and respective source regions on opposite sides of the sinker,

- wherein the first and second metal clamps are separated by a slot that extends between the parallel gate fingers, and

- a metal runner that extends in the slot between the separate metal clamps.

8. (Currently Amended) The transistor according to claim 7, wherein both gate fingers are connected to the associated metal runner at both their ends ~~**and at predetermined positions along their lengths**~~.

9. (Original) The transistor according to claim 7, wherein the metal runner is provided on a dielectric layer on top of the sinker.

10. (Original) The transistor according to claim 7, wherein each metal clamp covers the associated gate finger to shield it from a respective drain region.

11. (Original) The transistor according to claim 7, further comprising a well which extends from under the gate fingers and encloses said source regions wherein said well defines the channel.

12. (Cancelled)

13. (NEW) An RF power LDMOS transistor comprising:

- a substrate,
- a first and second source region spaced apart,
- a sinker separating said first and second source region,
- a first and second drain region arranged to define in combination with said first and second source region a first and second channel,
- a first and second gate finger covering said first and second channel, respectively, said gate fingers being interconnected by interconnection pieces,
- first and second metal clamps which short-circuit the sinker and respective source regions on opposite sides of the sinker,
- wherein the first and second metal clamps are separated by a slot that extends between the parallel gate fingers,
- a metal runner that extends in the slot between the separate metal clamps,
- a single metal layer, wherein said metal runner, said metal clamps, and interconnection pieces are formed in said single metal layer.

14. (NEW) The transistor according to claim 13, further comprising a first and second drain finger arranged above and coupled with said first and second drain region, respectively, wherein said drain fingers are formed in said single metal layer.

15. (NEW) The transistor according to claim 13, wherein both gate fingers are connected to the associated metal runner at both their ends.

16. (NEW) The transistor according to claim 13, wherein the metal runner is provided on a dielectric layer on top of the sinker.

17. (NEW) The transistor according to claim 13, wherein each metal clamp covers the associated gate finger to shield it from a respective drain region.

18. (NEW) The transistor according to claim 13, further comprising a well which extends from under the gate fingers and encloses said source regions wherein said well defines the channel.

19. (NEW) The transistor according to claim 13, wherein each source region comprise a first region and a second region surrounding said first region, wherein the second region is less doped than said first region.